WHAT IS CLAIMED IS:

1. A transceiver, comprising:

a plurality of pads, wherein at least one of said plurality of pads is a programmable IO pad capable of supporting at least two data protocols and at least two electrical specifications, wherein at least one of said plurality of pads is a programmable MDIO pad capable of supporting at least two data protocols and at least two electrical specifications; and

a plurality of ports in communications with said plurality of pads, wherein one of said plurality of ports is a parallel port in communications with said programmable IO pad.

2. The transceiver of claim 1, wherein said data protocols and electrical specifications comprise the standards specified in IEEE 802.3™ clause 45 and IEEE 802.3™ clause 22.

3. The transceiver of claim 1, wherein said data protocols include at least two of XGMII, TBI, RTBI data protocols, wherein said electrical specifications include at least two of HSTL, SSTL, and LVTTL electrical specifications.

4. The transceiver of claim 1, further comprise:

a bus structure for separating a power connection of said programmable MDIO pad from a power connection of said programmable IO pad.

5. The transceiver of claim 4, wherein said power connection of said programmable MDIO pad operates at a first voltage and said power connection of said programmable IO pad operates at a second voltage, wherein said first voltage differs from said second voltage.

6. The transceiver of claim 4, wherein said power connection of said programmable MDIO pad operates at 1.2 volts or 2.5 volts, and said power connection of said programmable IO pad operates at 2.5 volts or 3.3 volts.

7. The transceiver of claim 1, wherein said programmable IO pad is programmable to operate as an input or an output.

8. The transceiver of claim 1, wherein said programmable IO pad is programmable to receive or send at least one of a data signal and a clock signal.

9. The transceiver of claim 1, wherein one at least of said plurality of ports is a serial port in communications with said programmable IO pad.

10. The transceiver of claim 9, wherein said serial port is XAUI.

11. The transceiver of claim 9, further comprising a bus connecting said parallel port to said serial port on a common substrate with said plurality of ports.

12. The transceiver of claim 11, wherein said bus is configured to have a ring shape.

13. The transceiver of claim 11, wherein said bus is configured to have a ring shape around a logic core.

14. The transceiver of clam 11, further comprising a packet bit error rate tester (BERT) connected to said bus, said packet BERT able to determine bit error rates of at least one of said multiple parallel ports and said multiple serial ports.

15. A method for programming a transceiver, comprising:

accessing MDIO instructions that specify an electrical specification for the transceiver;

executing said MDIO instructions to configure a programmable IO pad disposed on the transceiver; and

sending or receiving data at said programmable IO pad in accordance with said electrical specification.

16. The method according to claim 15, further comprising:

receiving a signal from a pull-up or pull-down resistor to configure a programmable MDIO pad.

17. The method according to claim 16, further comprising:

configuring said programmable MDIO pad and said programmable IO pad to operate at different voltages.

18. The method according to claim 16, further comprising:

receiving a second signal from a pull-up or pull-down resister to configure a second programmable MDIO pad, wherein said second programmable MDIO pad is configured to support a different electrical specification or data protocol than the first programmable MDIO pad.

19. The method according to claim 15, further comprising:

receiving instructions from one or more management chips to communicate with the transceiver.